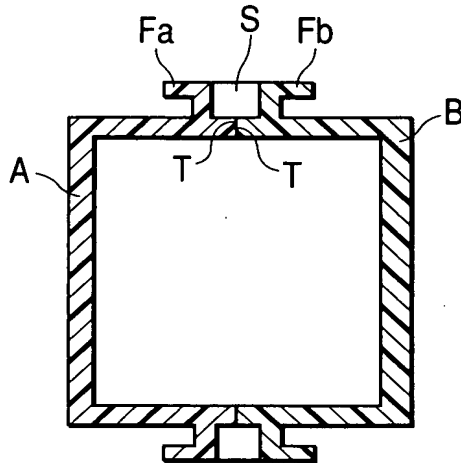
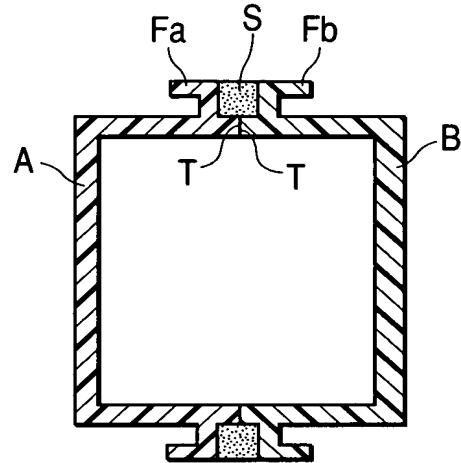




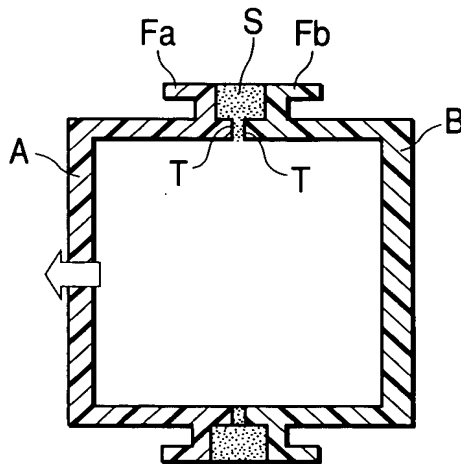
**FIG. 1A**



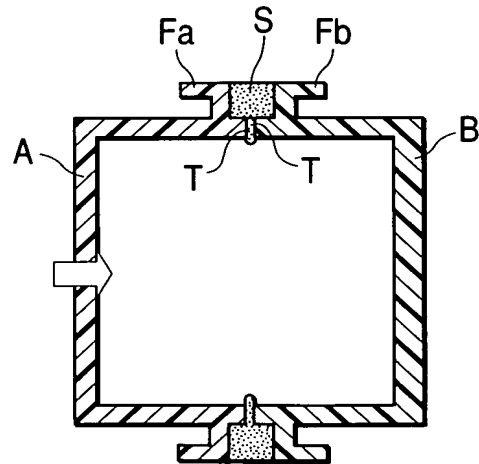
**FIG. 1B**



**FIG. 1C**



**FIG. 1D**



[illegible]

A cross-sectional view of a semiconductor device. The device consists of a substrate 20. A first conductive layer 21 is formed on the surface of the substrate 20. Two gate electrodes, labeled 31 and 32, are formed on top of the first conductive layer 21. Gate electrode 31 includes a side contact labeled C1. Both gate electrodes 31 and 32 are electrically connected to a common power supply terminal labeled P.

FIG. 3B

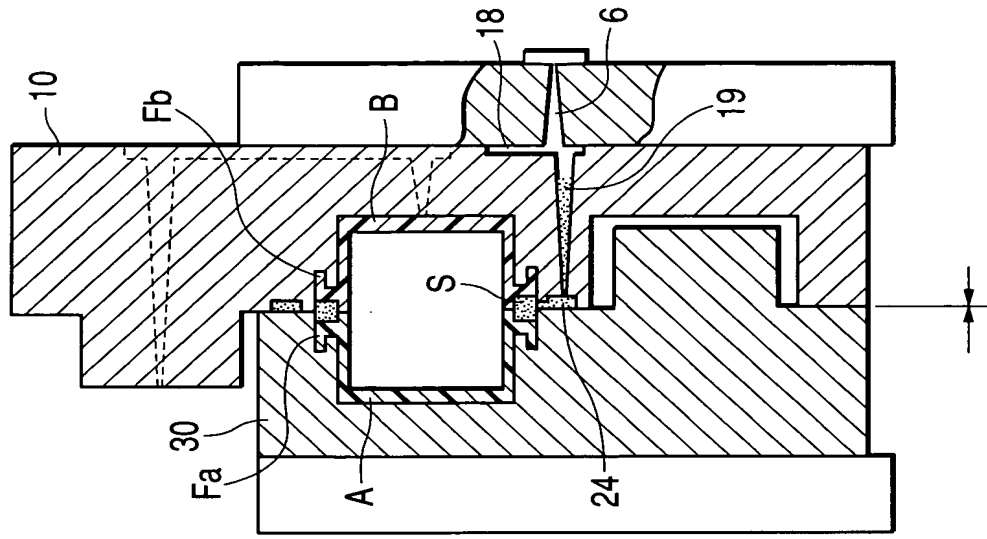


FIG. 3A

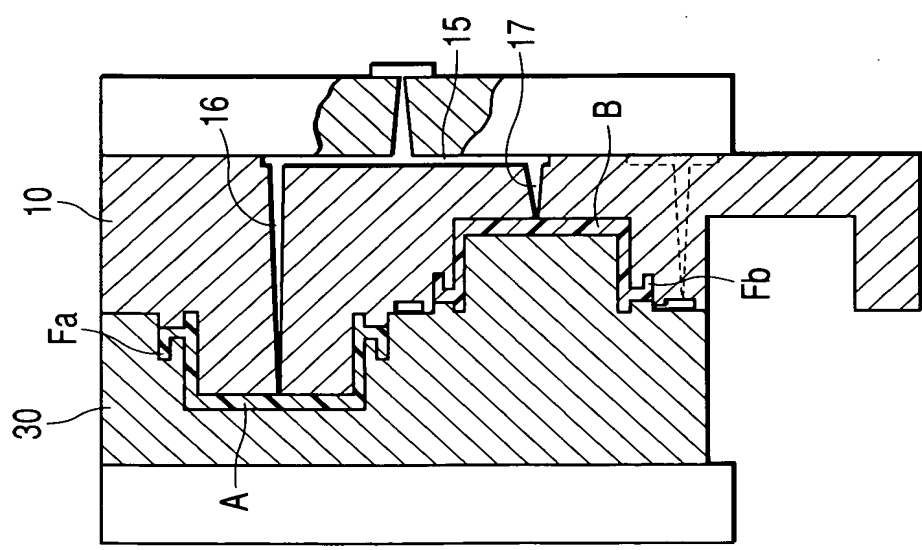
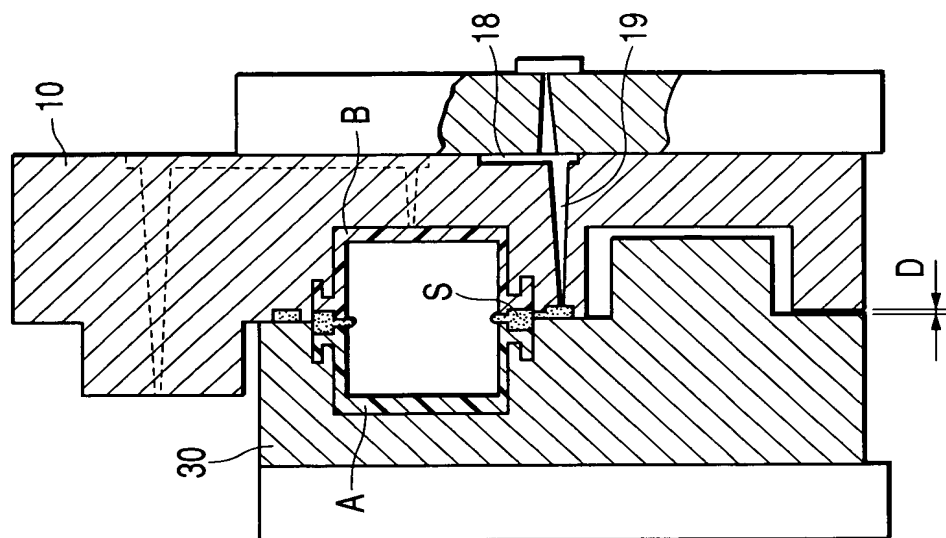
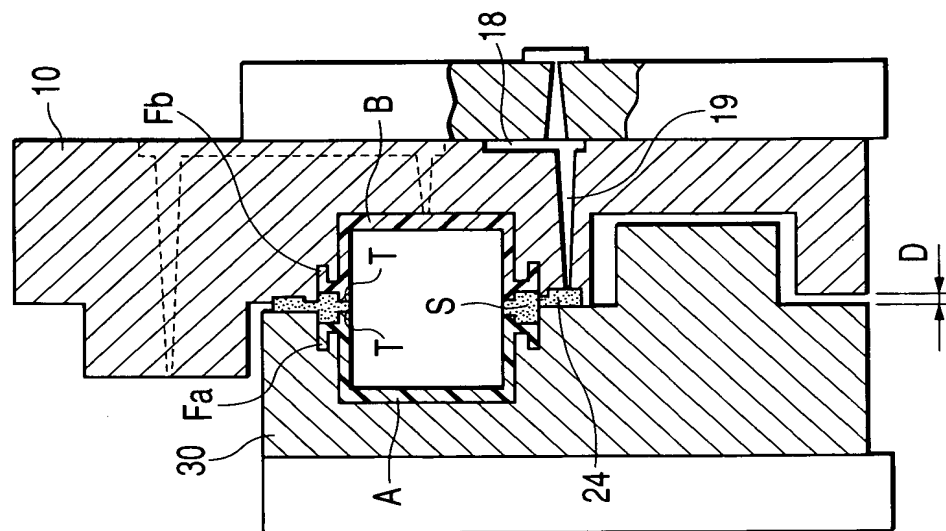


FIG. 4B



CLOSE  
MOLD AGAIN

FIG. 4A



OPEN  
MOLD

FIG. 5A

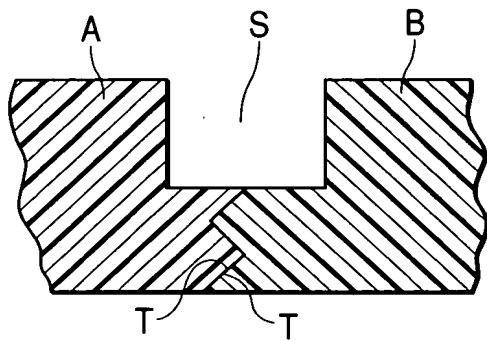


FIG. 5B

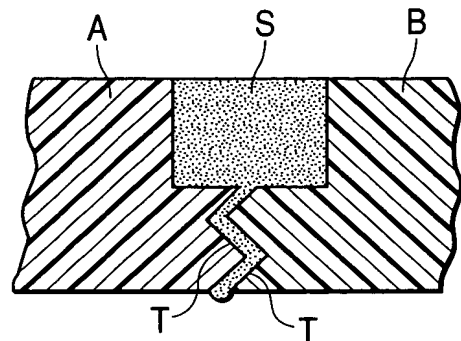


FIG. 5C

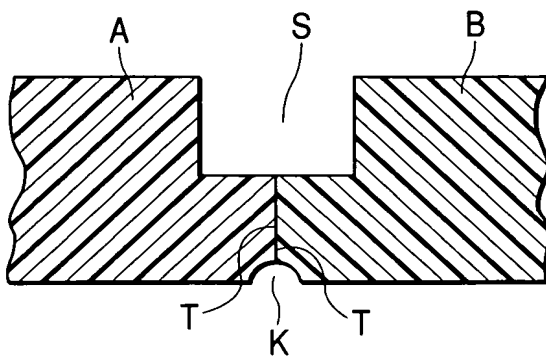


FIG. 5D

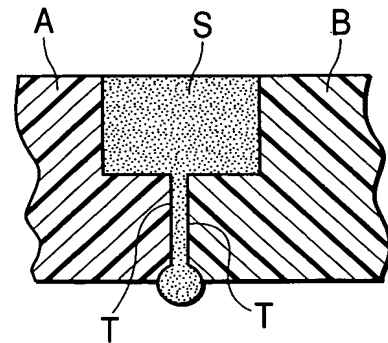


FIG. 6A

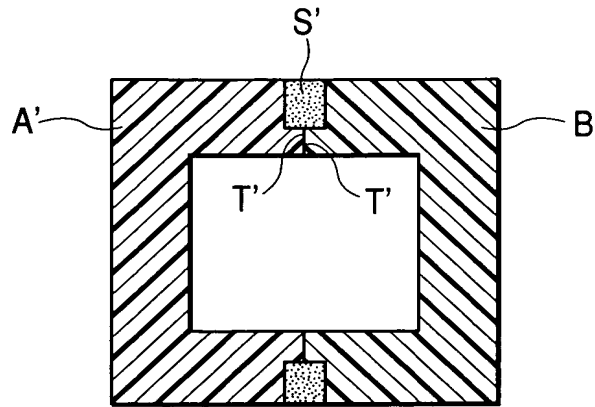


FIG. 6B

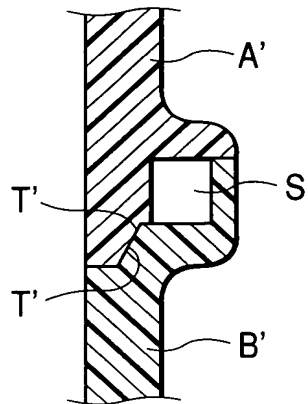


FIG. 6C

